



MK6604

Complementary Enhancement Mode Field Effect Transistor

N-Channel

V(BR)DSS	RDS(on)MAX	ID
20 V	40mΩ@ 4.5V	3.4A
	50mΩ@ 2.5V	

P-Channel

V(BR)DSS	RDS(on)MAX	ID
-20	90mΩ@ -4.5V	-2.5A
	115mΩ@ -2.5V	

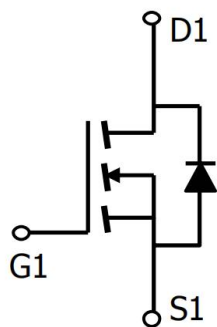
FEATURE:

※ TrenchFET Power MOSFET

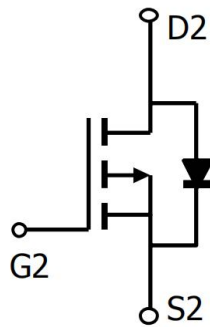
MARKING:

F4CA-MK

Equivalent Circuit:



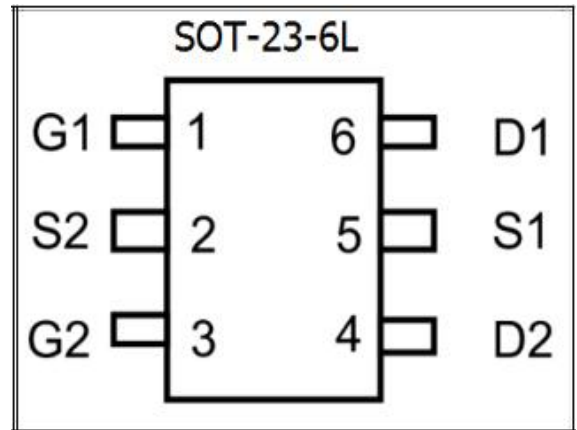
n-channel



p-channel

General Description:

The MK6604 uses advanced trench technology to provide excellent RDS(ON) and low gate charge. The complementary MOSFETs form a high-speed power inverter, suitable for a multitude of applications. Standard Product MK6604 is Pb-free (meets ROHS & Sony 259 specifications).



Maximum ratings (Ta=25°C unless otherwise noted)

Parameter	Symbol	Max n-channel	Max P-channel	Unit
Drain-Source Voltage	VDS	20	-20	V
Gate-Source Voltage	VGS	±8	±8	
Continuous Drain Current	ID	3.4	-2.5	A
Pulsed Diode Curren	IDM	13	-13	
Continuous Source-Drain Current(Diode Conduction)	IS	1.5	-1.5	
Power Dissipation	PD	1.1	1.1	W
Thermal Resistance from Junction to Ambient (t≤10s)	RθJA	125	125	°C/W
Operating Junction	TJ	150	150	°C
Storage Temperature	TSTG	-55~+150	-55~+150	°C



N-channel

N-channel MOSFET Electrical Characteristics (Ta = 25 °C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-source breakdown voltage	V(BR)DSS	VGS = 0V, ID = 250μA	20			V
Gate-source threshold voltage	VGS(th)	VDS =VGS, ID = 250μA	0.4		1	V
Gate-body leakage current	IGSS	VDS =0V, VGS = ±8V			±100	nA
Zero gate voltage drain current	IDSS	VDS = 20V, VGS =0V			1	μA
Static Drain-Source On-Resistance	RDS(on)	VGS = 4.5V, ID = 2.8A		25	40	mΩ
		VGS = 2.5V, ID = 2A		37	50	mΩ
Forward transconductance	gfs	VDS = 5V, ID = 3.4A		16		S
Diode forward voltage	VSD	IS= 1A,VGS=0V		0.8	1.2	V
Maximum Body-Diode Continuous Current	IS				1.5	A
Dynamic						
Input capacitance	Ciss	VDS = 10V, VGS =0V, f=1MHz		260		pF
Output capacitance	Coss			48		pF
Reverse transfer capacitance	Crss			27		pF
Total gate charge	Qg	VDS = 10V, VGS = 4.5V, ID = 3.4A		2.9		nC
Gate-source charge	Qgs			0.4		nC
Gate-drain charge	Qgd			0.6		nC
Gate resistance	Rg	f=1MHz		3		Ω
Switching						
Turn-on delay time	td(on)	VDS= 10V RL=3Ω, ID =3.4A, VGS= 4.5V,Rg=6Ω		2.5		ns
Rise time	tr			3.2		ns
Turn-off delay time	td(off)			21		ns
Fall time	tf			3		ns
Body Diode Reverse Recovery Time	Trr	IF=3.4A, dI/dt=100A/μs		14		ns
Body Diode Reverse Recovery Charge	Qrr	IF=3.4A, dI/dt=100A/μs		3.8		nC

Note :

1. Repetitive Rating : Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t < 10 sec.
3. Pulse Test : Pulse Width≤300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production testing.



P-channel

P-channel MOSFET Electrical Characteristics (Ta = 25 °C Unless Otherwise Noted)

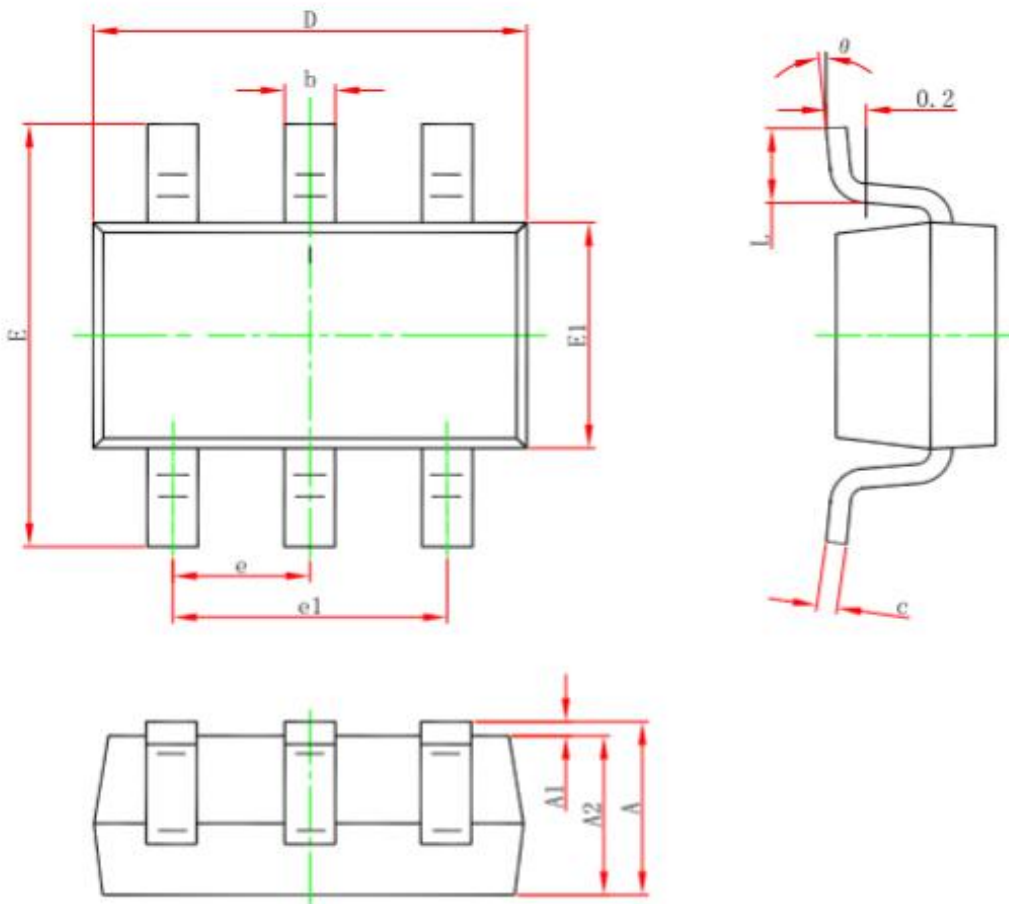
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-source breakdown voltage	V(BR)DSS	VGS = 0V, ID = -250μA	-20			V
Gate-source threshold voltage	VGS(th)	VDS =VGS, ID = -250μA	-0.4		-1	V
Gate-body leakage current	IGSS	VDS =0V, VGS = ±8V			±100	nA
Zero gate voltage drain current	IDSS	VDS = -20V, VGS =0V			-1	μA
Static Drain-Source On-Resistance	RDS(on)	VGS = -4.5V, ID = -2.8A		69	90	mΩ
		VGS = -2.5V, ID = -2A		93	115	mΩ
Forward transconductance	gfs	VDS = -5V, ID = -2.5A		13		S
Diode forward voltage	VSD	IS= -1A,VGS=0V		-0.8	-1.2	V
Maximum Body-Diode Continuous Current	IS				-1.5	A
Dynamic						
Input capacitance	Ciss	VDS = -10V, VGS =0V, f=1MHz		560		pF
Output capacitance	Coss			80		pF
Reverse transfer capacitance	Crss			70		pF
Total gate charge	Qg	VDS = -10V, VGS = -4.5V, ID = -2.5A		8.5		nC
Gate-source charge	Qgs			1.2		nC
Gate-drain charge	Qgd			2.1		nC
Gate resistance	Rg	f=1MHz		15		Ω
Switching						
Turn-on delay time	td(on)	VDS= -10V RL= 4Ω, ID = -2.5A, VGS= -4.5V,Rg=6Ω		7.2		ns
Rise time	tr			36		ns
Turn-off delay time	td(off)			53		ns
Fall time	tf			56		ns
Body Diode Reverse Recovery Time	Trr	IF= -2.5A, dI/dt=100A/μs		37		ns
Body Diode Reverse Recovery Charge	Qrr	IF= -2.5A, dI/dt=100A/μs		27		nC

Note :

1. Repetitive Rating : Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t < 10 sec.
3. Pulse Test : Pulse Width≤300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production testing.



SOT-23-6L PACKAGE OUTLINE DIMENSIONS:



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E1	1.500	1.700	0.059	0.067
E	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
theta	0°	8°	0°	8°



N-channel Typical Electrical AND Thermal Characteristics:

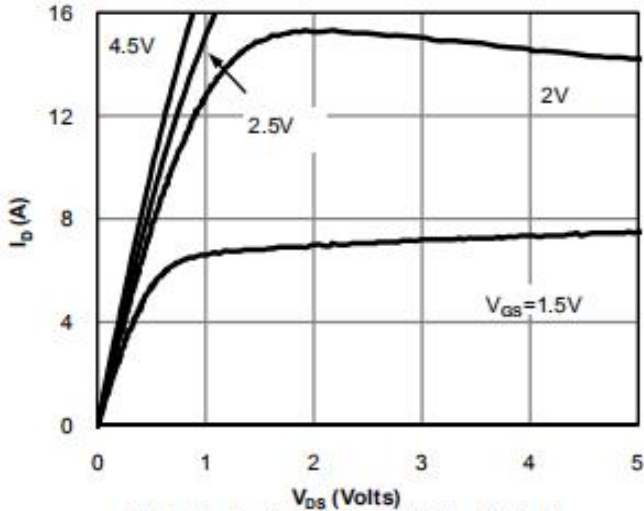


Fig 1: On-Region Characteristics (Note E)

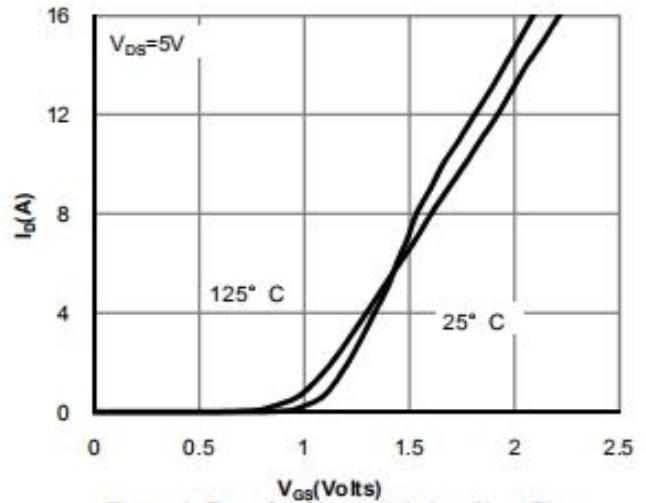


Figure 2: Transfer Characteristics (Note E)

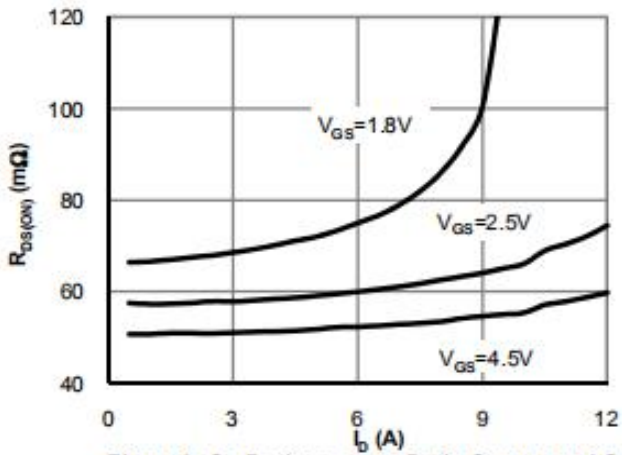


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

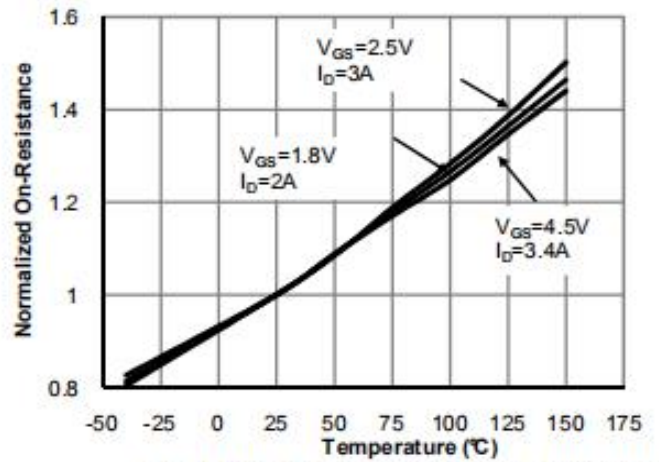


Figure 4: On-Resistance vs. Junction Temperature (Note E)

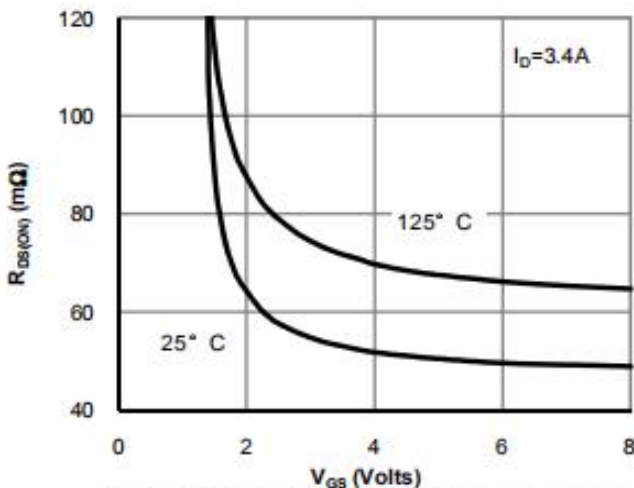


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

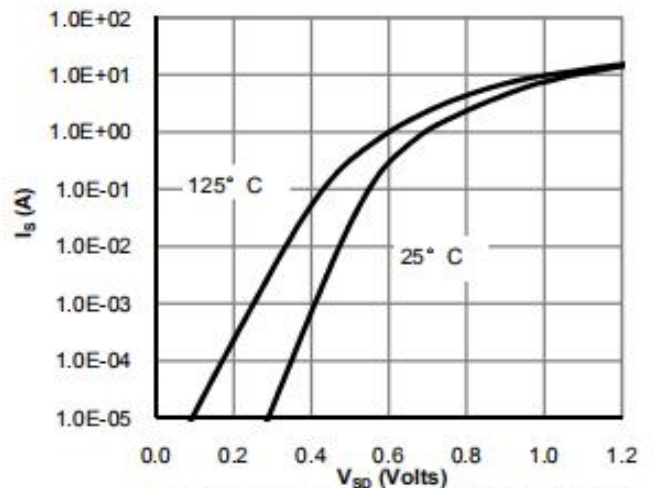


Figure 6: Body-Diode Characteristics (Note E)



N-channel Typical Electrical AND Thermal Characteristics:

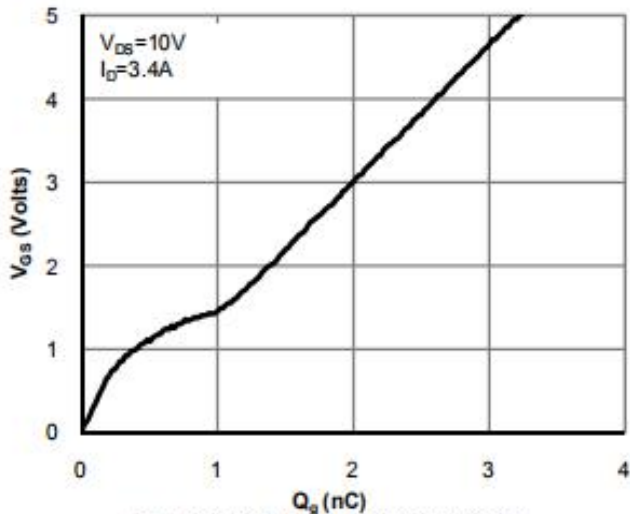


Figure 7: Gate-Charge Characteristics

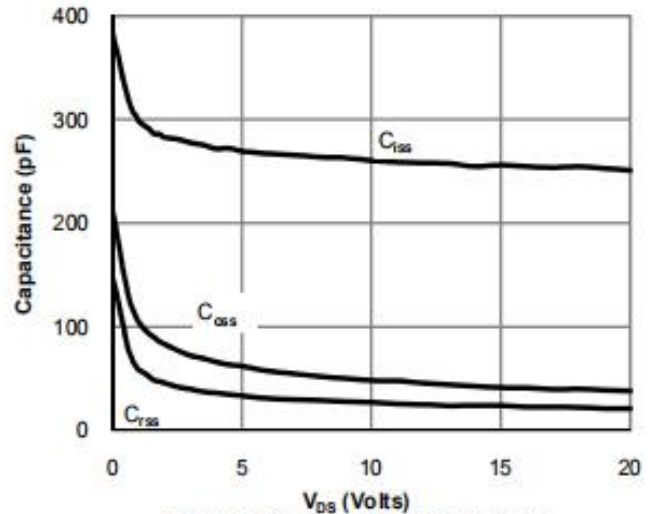


Figure 8: Capacitance Characteristics

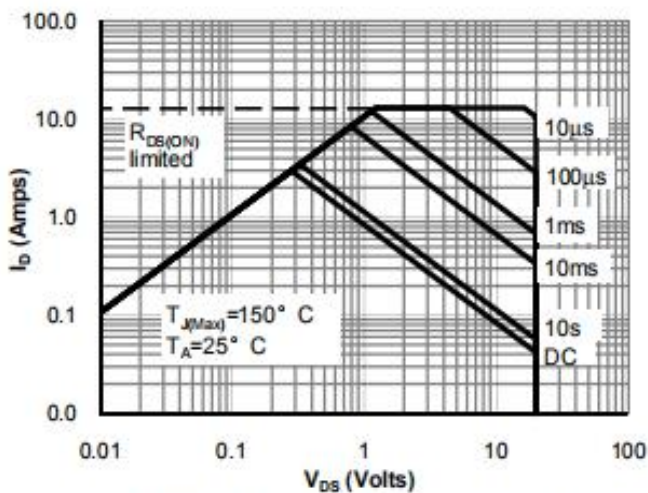


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

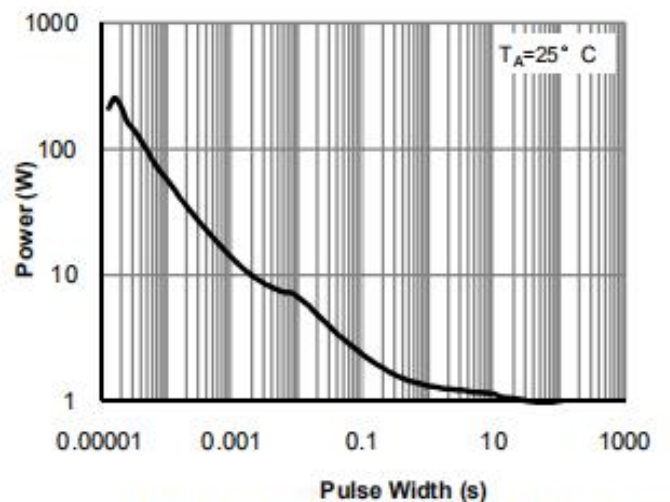


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

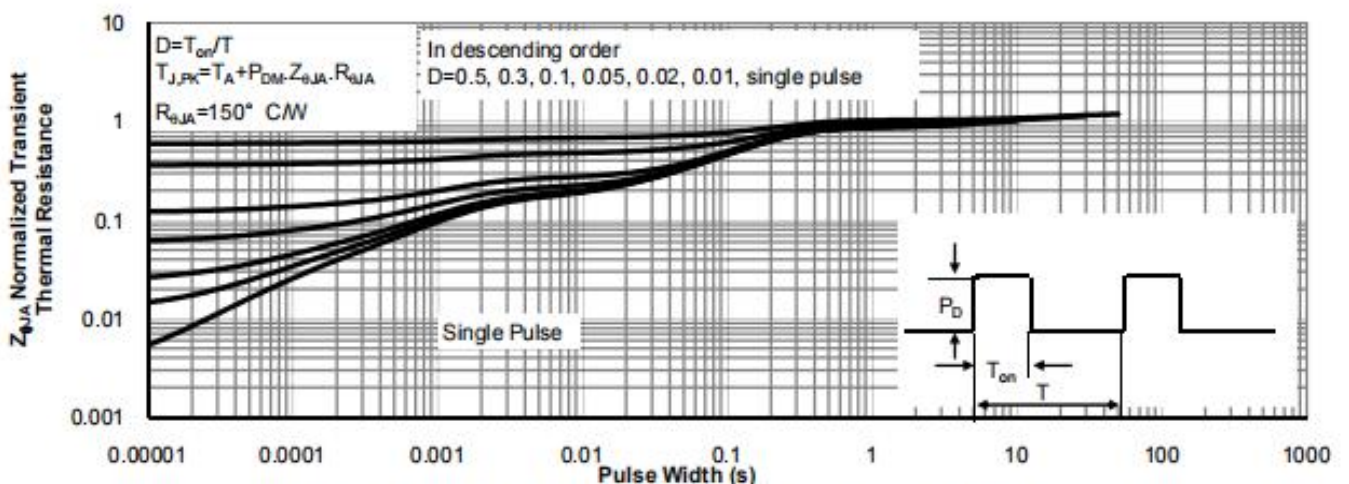


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)



P-channel Typical Electrical AND Thermal Characteristics:

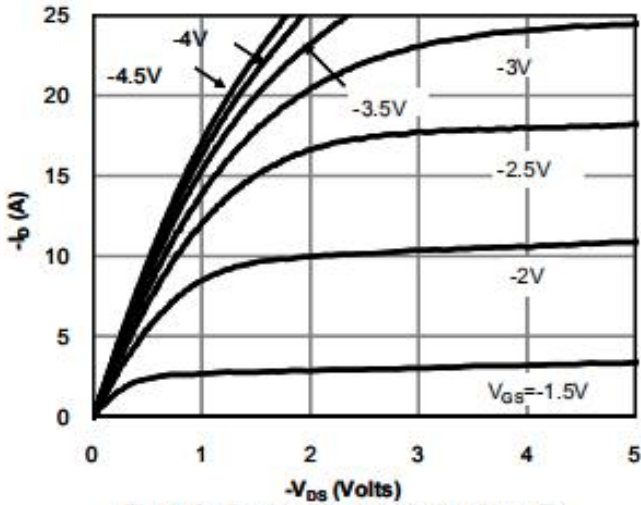


Fig 1: On-Region Characteristics (Note E)

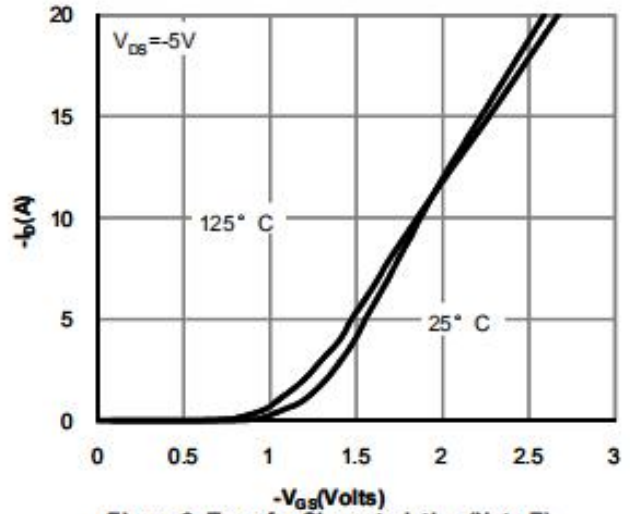


Figure 2: Transfer Characteristics (Note E)

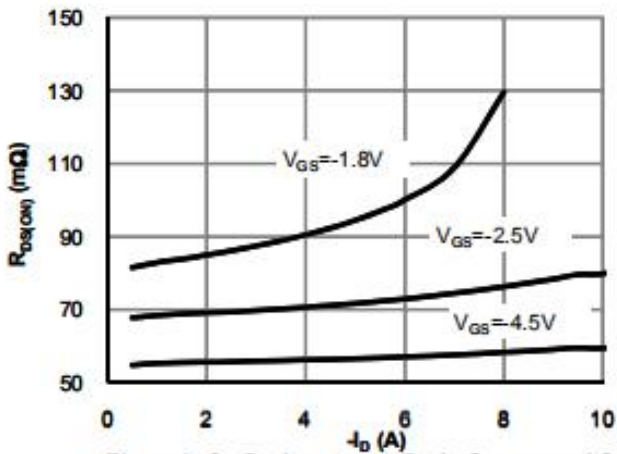


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

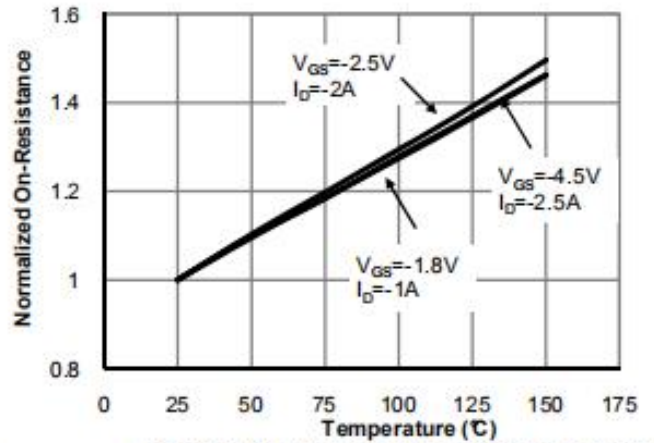


Figure 4: On-Resistance vs. Junction Temperature (Note E)

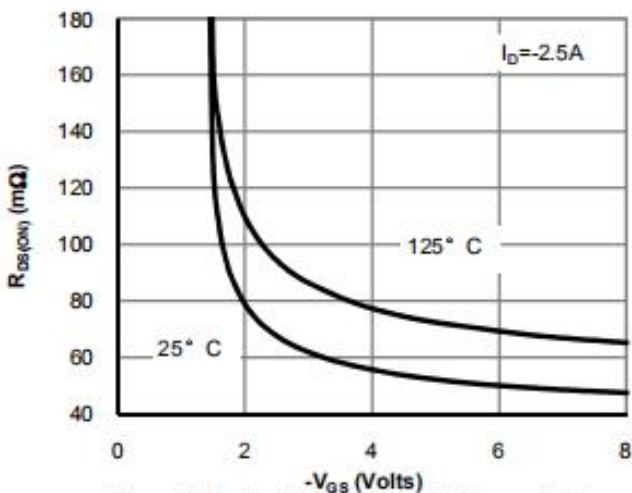


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

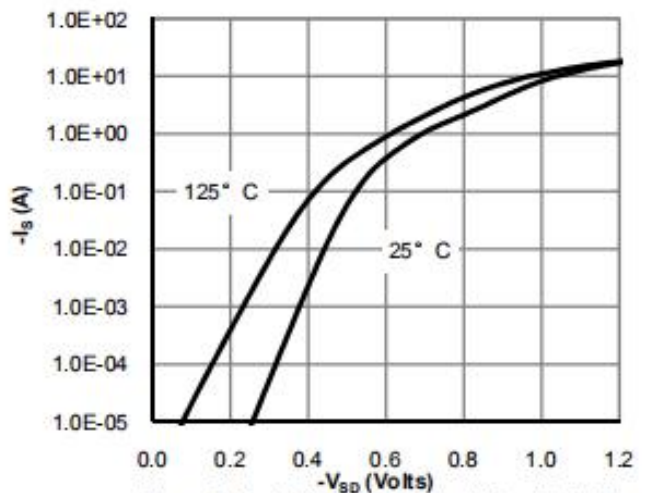


Figure 6: Body-Diode Characteristics (Note E)



P-channel Typical Electrical AND Thermal Characteristics:

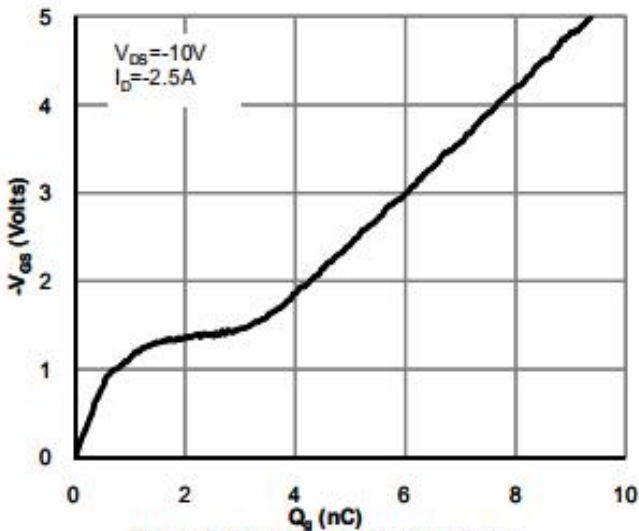


Figure 7: Gate-Charge Characteristics

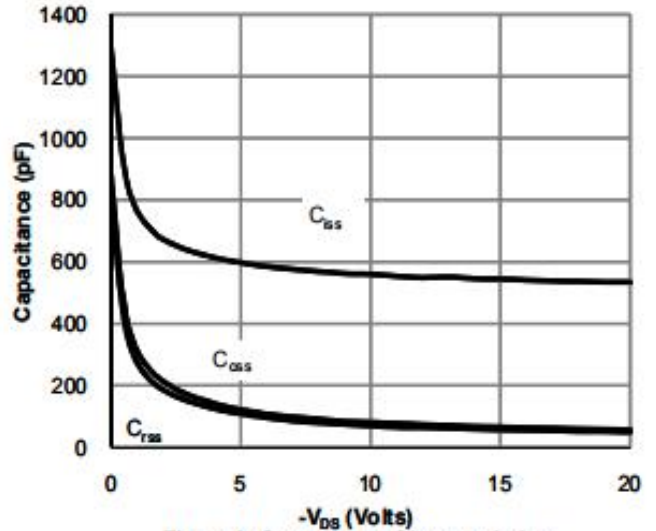


Figure 8: Capacitance Characteristics

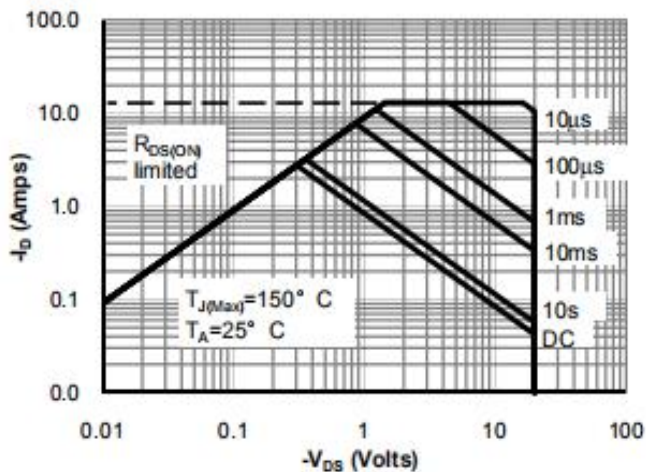


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

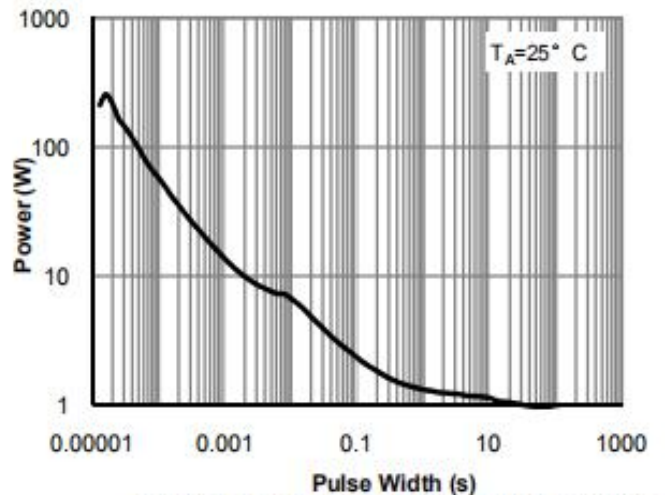


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note F)

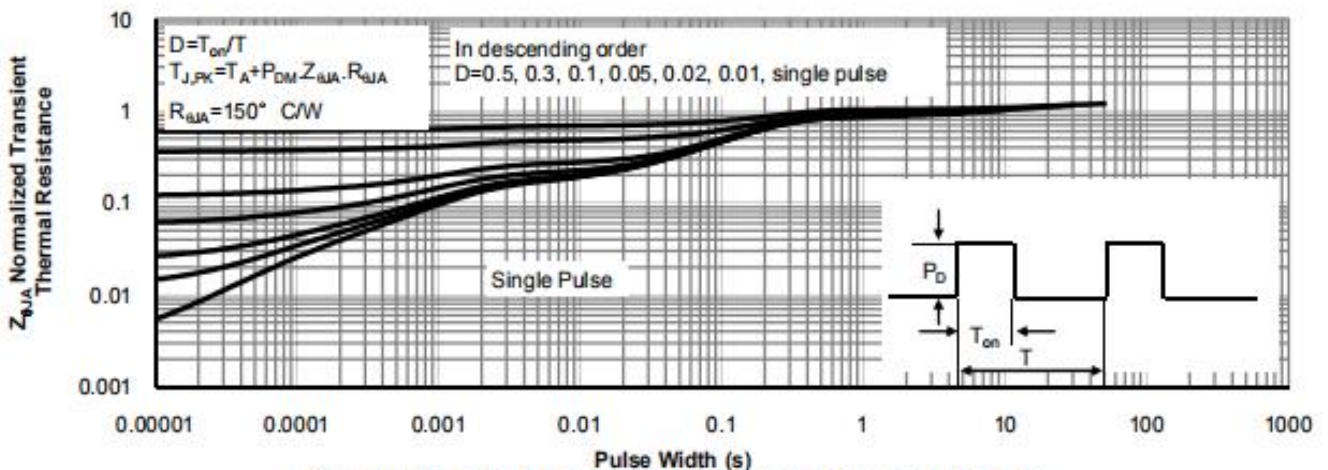


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)